GEETHANJALI COLLEGE OF ENGINEERING AND TECHNOLOGY(AUTONOMOUS)
Cheeryal (V), Keesara (M), R.R. Dist., - 501301, Telangana State

Department of Electronics and Communication Engineering

M.Tech Program in VLSI System Design

Vision

To impart quality technical education in Electronics and Communication Engineering emphasizing analysis, design/synthesis and evaluation of hardware/ embedded software, using various Electronic Design Automation (EDA) tools with accent on creativity, innovation and research thereby producing competent engineers who can meet global challenges with societal commitment.

Mission

- To impart quality education in fundamentals of basic sciences, mathematics, electronics and communication engineering through innovative teaching-learning processes.
- To facilitate Graduates define, design, and solve engineering problems in the field of Electronics and Communication Engineering using various Electronic Design Automation (EDA) tools.
- To encourage research culture among faculty and students thereby facilitating them to be creative and innovative through constant interaction with R & D organizations and Industry.
- To inculcate teamwork, imbibe leadership qualities, professional ethics and social responsibilities in students and faculty.

Program Educational Objectives of M.Tech (VLSI System design) Program:

1. To impart knowledge of VLSI / Nanometer scale IC Design using different software tools
2. To provide hands-on design capabilities for Analog, Digital and Mixed signal ICs.
3. To inculcate positive attitude and provide effective communication skills to take upresearch and development work in the field of VLSI system design.

Program Outcomes of M.Tech (VLSI System design) Program:

1. Able to design and evaluate VLSI Systems.
2. Able to design, analyze, and testing of VLSI circuits using different design tools.
3. Able to apply knowledge from the program and other disciplines to identify, formulate,solve novel advanced electronics engineering problems
4. Able to understand and integrate new knowledge within the field.
5. Able to apply advanced technical knowledge in multiple contexts
6. Able to understand and design advanced VLSI systems (Both Analog and Digital Systems) and simulate the performance, analyze and interpret data.
7. Able to convey technical material through formal written reports which satisfy acceptedstandards of writing style.

8. Able to demonstrate effective communication skills in oral, written and electronic media.
9. Able to become knowledgeable about contemporary developments in the field of VLSIsystems.
10. Continue to improve their professional skills through lifelong learning

Geethanjali College of Engineering and Technology (GCET)

(AUTONOMOUS)

GCET M. Tech Academic Regulations w.e.f. 2016-17

ACADEMIC REGULATIONS 2016 for CBCS Based M.Tech. (Regular) Programmes

(Effective for the students admitted into I year from the Academic Year **2016-17** and onwards)

1.0 Post-Graduate Degree (M. Tech) Programmes in Engineering:

GCET offers 2 Year (4 Semesters) full-time **Master of Technology** (M.Tech.) Degree programmes, under Choice Based Credit System (CBCS) at GCET Hyderabad with effect from the Academic Year 2016 - 17 onwards in the different branches of Engineering with different specializations.

2.0 Eligibility for Admission:

2.1 Admission to the M. Tech programme shall be made either on the basis of the Rank/Percentile earned by the candidate in the relevant qualifying GATE Examination / the Merit Rank obtained by the qualifying candidate at an Entrance Test conducted by the Telangana State Government (PGECET) for M.Tech. Programmes / an Entrance Test conducted by the Jawaharlal Nehru Technological University Hyderabad / on the basis of any other order of merit approved by the University, subject to reservations as prescribed by the Government from time to time.

2.2 The medium of instructions for all M. Tech programmes shall be ENGLISH only.

3.0 M.Tech. Programme Structure:

3.1 The M.Tech. Programmes of GCET are of Semester Pattern, with 4 Semesters constituting 2 Academic Years, each Academic Year having TWO Semesters (First/Odd and Second/Even Semesters). Each Semester shall be of 21 Weeks duration (inclusive of Examinations), with a minimum of 90 Instructional Days per Semester.

3.2 UGC/ AICTE specified Definitions/ Descriptions are adopted appropriately for various terms and abbreviations used in these M. Tech Programmes - Academic Regulations.

3.2.1 Semester Scheme:

Each Semester having - 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) as denoted are taken as 'references' for the present set of Regulations. The terms 'SUBJECT' or

'COURSE' imply the same meaning here, and refer to 'Theory Subject', or 'Lab Course', or 'Design/ Drawing Subject', or 'Seminar', or 'Comprehensive Viva', or 'Project', as the case may be.

3.2.2 Credit Courses:

All Subjects (or Courses) are to be registered by a student in a Semester to earn Credits. Credits shall be assigned to each Subject/ Course in a L: T: P: C (Lecture Periods: Tutorial Periods: Practicals Periods : Credits) Structure, based on the following general pattern …

• One hour/ Week/ Semester for Theory/ Lecture (L) Courses; and,

• Two hours/ Week/ Semester for Laboratory/ Practical (P) Courses or Tutorials (T).

Other student activities like Study Tour, Guest Lecture, Conference/ Workshop Participations, Technical Paper Presentations etc., and identified Mandatory Courses if any, will not carry Credits.

3.2.3 Subject/ Course Classification:

All Subjects/ Courses offered for the M. TECH are broadly classified as : (a) Core Courses (CoC), and (b) Elective Courses (Eℓ C).

- Core Courses (CoC) and Elective Courses (Eℓ C) are categorized as PS (Professional Subjects), which are further subdivided as – (i) PC (Professional/ Departmental Core) Subjects, (ii) PE (Professional/ Departmental Electives) , (iii) Seminar, (iv) Comprehensive Viva, and (v) Project Work (PW).

3.2.4 Course Nomenclature:

The Curriculum Nomenclature or Course-Structure Grouping for the M.Tech. Degree Programmes is as listed below …

S.No	***Broad Course Classification***	***Course Group/ Category***	***Courses Description***	***Credits***
1)	Core Courses (CoC)	PC- Professional Core	Includes core subjects related to the Parent Discipline/ Department/ Branch of Engg.	20
2)	Elective Courses (EℓC)	PE– Professional Electives	Includes Elective subjects related to the Parent Discipline/ Department/ Branch of Engg.	32
3)	Core Courses	Project Work	M.Tech. Project or PG Project or PG Major Project	30
		Seminar	Seminar/ Colloquium based on core contents related to Parent Discipline/ Department/ Branch of Engg.	2
		Comprehensive Viva-voce	Viva-voce covering all the PG Subjects and related aspects	4
		Communication Skills/ Soft Skills	Lab oriented	2
Total Credits				**90**

4.0 Course Work:

4.1 A Student, after securing admission, shall pursue and complete the M.Tech. M. TECH in a minimum period of 2 Academic Years (4 Semesters), and within a maximum period of 4 Academic Years (starting from the Date of Commencement of I Year).

4.2 Each student shall Register for and Secure the specified number of Credits required for the completion of the M. Tech programme and Award of the M.Tech. Degree in respective Branch of Engineering with the chosen Specialization.

4.3 I Year is structured to provide typically 28 Credits (28 C) in each of the I and II Semesters, and II Year comprises of 34 Credits (34 C), totaling to 90 Credits (90 C) for the entire M.Tech. Programme.

5.0 Course Registration:

5.1 A 'Faculty Advisor' shall be assigned to each M.Tech. Programme with respective Specialization, who will advise the Students about the M.Tech. Programme Specialization, its Course Structure and Curriculum, Choice/ Option for Subjects/ Courses, based on his competence, progress, pre-requisites and interest.

5.2 A Student may be permitted to Register for Subjects/ Courses of 'his CHOICE' with a typical total of 28 Credits per Semester in I Year (Minimum being 24 C and Maximum being 32 C, permitted deviation being ± 15%), and 16 Credits (inclusive of Project) per III Semester in II Year (Minimum being 16 C and Maximum being 32 C), 18 credits (inclusive of Project) per IV Semester in II Year (minimum being 18 C and maximum 32 C), based on his interest, competence, progress, and 'PRE-REQUISITES' as indicated for various Subjects/ Courses, in the Department Course Structure (for the relevant Specialization) and Syllabus contents for various Subjects/ Courses.

5.3 Choice for 'additional Subjects/ Courses' in any Semester (above the typical 28/16/18 Credit norm, and within the Maximum Permissible Limit of 32/32 Credits, during I/ II Years as applicable) must be clearly indicated in the Registration, which needs the specific approval and signature of the Faculty Advisor/ Counselor on hard-copy.

5.4 Dropping of Subjects/ Courses in any Semester of I Year may be permitted, ONLY AFTER obtaining prior approval and signature from the Faculty Advisor (subject to retaining a minimum of 24 Credits), 'within 15 Days of Time' from the beginning of the current Semester.

6.0 Attendance Requirements:

6.1 A Student shall be eligible to appear for the End Semester Examination (SEE) of any Subject, if he acquires a minimum of 75% of attendance in that Subject for that Semester.

6.2 A Student's Seminar Report and Seminar Presentation shall be eligible for evaluation, only if he ensures a minimum of 75% of his attendance in Seminar Presentation Classes during that Semester.

6.3 Condoning of shortage of attendance up to 10% (65% and above, and below 75%) in each Subject or Seminar of a Semester may be granted by the College Academic Council on genuine and valid grounds, based on the Student's representation with supporting evidence.

6.4 A stipulated fee per Subject/Seminar shall be payable towards condoning of shortage of attendance.

6.5 Shortage of Attendance below 65% in any Subject/Seminar shall in NO case be condoned.

6.6 A Student, whose shortage of attendance is not condoned in any Subject(s) or Seminar in any Semester, is considered as 'Detained in that Subject(s)/Seminar', and is not eligible to take End Examination(s) of such Subject(s) (and in case of Seminars, his Seminar Report or Presentation are not eligible for evaluation) in that Semester; and he has to seek Re-registration for those Subject(s)/Seminar in subsequent Semesters, and attend the same as and when offered.

7.0 Academic Requirements:

The following Academic Requirements have to be satisfied, in addition to the Attendance Requirements mentioned in Item No. 6**.**

7.1 A Student shall be deemed to have satisfied the Academic Requirements and earned the Credits allotted to each Subject/ Course, if he secures not less than 40% Marks (28 out of 70 Marks) in the End Semester Examination, and a minimum of 50% of Marks in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades, this implies securing B Grade or above in that Subject.

7.2 A Student shall be deemed to have satisfied the Academic Requirements and earned the Credits allotted to - Seminar, and Comprehensive Viva-voce, if he secures not less than 50% of the total marks to be awarded for each. The Student would be treated as failed, if he - (i) does not attend the

Comprehensive Viva-voce as per the schedule given, or (ii) does not present the Seminar as required, or (ii) secures less than 50% of Marks (< 50 Marks) in Seminar/ Comprehensive Viva-voce evaluations. He may reappear for comprehensive viva where it is scheduled again; For seminar, he has to reappear in the next subsequent Semesters, as and when scheduled.

7.3 A Student shall - register for all Subjects covering 90 Credits as specified and listed in the Course Structure for the chosen M. TECH Specialization, put up all the Attendance and Academic requirements for securing 90 Credits obtaining a minimum of B Grade or above in each Subject, and 'earn all 90 Credits securing SGPA ≥ 5.0 (in each Semester) and final CGPA (ie., CGPA at the end of M. TECH) ≥ 5.0, to successfully complete the M. TECH.

7.4 Marks and Letter Grades obtained in all those Subjects covering the above specified 90 Credits alone shall be considered for the calculation of final CGPA, which shall be indicated in the Grade Card of II Year II Semester.

7.5 If a student registers for some more 'extra Subjects' (in the parent Department or other Departments/Branches of Engg.) other than those listed Subjects totaling to 90 Credits as specified in the Course Structure, the performances in those 'extra Subjects' (although evaluated and graded using the same procedure as that of the required 90 Credits) will not be taken into account while calculating the SGPA and CGPA. For such 'extra Subjects' registered, % marks and Letter Grade alone will be indicated in the Grade Card, as a performance measure, subject to completion of the Attendance and Academic Requirements as stated in Items 6 and 7.1 – 7.4 above.

7.6 Students who fail to earn 90 Credits as per the specified Course Structure, and as indicated above, within 4 Academic Years from the Date of Commencement of their I Year, shall forfeit their seats in M.Tech. Programme and their admissions shall stand cancelled.

7.7 When a Student is detained due to shortage of attendance in any Subject(s)/Seminar in any Semester, no Grade Allotment will be done for such Subject(s)/Seminar, and SGPA/ CGPA calculations of that Semester will not include the performance evaluations of such Subject(s)/Seminar in which he got detained. However, he becomes eligible for re-registration of such Subject(s)/Seminar (in which he got detained) in the subsequent Semester(s), as and when next offered, with the Academic Regulations of the Batch into which he gets readmitted, by

paying the stipulated fees per Subject. In all these re-registration cases, the Student shall have to secure a fresh set of Internal Marks (CIE) and End Semester Examination Marks (SEE) for performance evaluation in such Subject(s), and subsequent SGPA/ CGPA calculations.

7.8 A Student eligible to appear in the End Semester Examination in any Subject, but absent at it or failed (failing to secure B Grade or above), may reappear for that Subject at the supplementary examination (SEE) as and when conducted. In such cases, his Internal Marks (CIE) assessed earlier for that Subject/ Course will be carried over, and added to the marks to be obtained in the supplementary examination (SEE), for evaluating his performance in that Subject.

8.0 Evaluation - Distribution and Weightage of Marks:

8.1 The performance of a Student in each Semester shall be evaluated Subject-wise (irrespective of Credits assigned) with a maximum of 100 Marks for Theory or Practicals or Seminar or Drawing/Design or Comprehensive Viva-voce etc;

however, the M.Tech. Project Work (Major Project) will be evaluated for 200 Marks.

8.2 a) For Theory Subjects, CIE Marks shall comprise of - Mid-Term Examination Marks (for 25 Marks), and Assignment Marks (for 5 Marks).

b) During the Semester, there shall be 2 Mid-Term examinations. Each Mid-Term examination shall be for 25 Marks (with 120 minutes duration). The AVERAGE performance out of these two Mid-Term Examinations shall be considered for the award of 25 Marks.

8.3 For Practical Subjects, there shall be a Continuous Internal Evaluation (CIE) during the Semester for 30 Internal Marks, and 70 Marks are assigned for Lab./Practicals End Semester Examination (SEE). Out of the 30 Marks for Internals, day-to-day work assessment in the laboratory shall be evaluated for 20 Marks; and the performance in an internal Lab./Practical Test shall be evaluated for 10 marks. The SEE for Lab./ Practicals shall be conducted at the end of the Semester by the concerned Lab. Teacher and another faculty member of the same Department as assigned by the Head of the Department.

8.4 There shall be a Seminar Presentation in I Year I Semester or II Semester.

For the Seminar, the Student shall collect the information on a specialized topic, prepare a Technical Report and submit to the Department at the time of Seminar Presentation. The Seminar Presentation (along with the Technical Report) shall be evaluated by Two Faculty

Members assigned by Head of the Department, for 100 Marks. There shall be no SEE or External Examination for Seminar.

8.5 Each Student shall appear for a Comprehensive Viva-Voce at the end of the III Semester (II Year I Semester). The Comprehensive Viva-Voce shall be conducted by a Committee, consisting of three senior faculty members of Department nominated by the Head of the Department, and the performance evaluation shall be for 100 Marks. There are no Internal Marks for the Comprehensive Viva-voce.

8.6 a) Every Student shall be required to execute his M.Tech. Project, under the guidance of the Supervisor assigned to him by the Head of Department. The Project shall start immediately after the completion of the I Year II Semester, and shall continue through II Year I and II Semesters. The Student shall carry out the literature survey, select an appropriate topic and submit a Project Proposal within 6 weeks (immediately after his I Year II Semester End Examinations), for approval by the Project Review Committee (PRC). The PRC shall be constituted by the Head of Department, and shall consist of the Head of Department, Project Supervisor, and a Senior Faculty Member of the Department. The Student shall present his Project Work Proposal to the PRC (PRC-I Presentation), on whose approval he can 'REGISTER for the PG Project'. Every Student must compulsorily register for his M.Tech. Project Work, within the 6 weeks of time-frame as specified above. After Registration, the Student shall carry out his work, and continually submit 'a fortnightly progress report' to his Supervisor throughout the Project period. The PRC will monitor the progress of the Project Work and review, through PRC-II and PRC-III Presentations – one at the end of the II Year I Semester, and one before the submission of M.Tech. Project Work Report/ Dissertation.

b) After PRC-III presentation, the PRC shall evaluate the entire performance of the Student and declare the Project Report as 'Satisfactory' or 'Unsatisfactory'. Every Project Work Report/ Dissertation (that has been declared 'satisfactory') shall undergo 'Plagiarism Check' as per the University/ College norms to ensure content plagiarism below a specified level of 30%, and to become acceptable for submission. In case of unacceptable plagiarism levels, the student shall resubmit the Project Work Report, after carrying out the necessary modifications/ additions to his Project Work/ Report as per his Supervisor's advice, within the specified time, as suggested by the PRC.

c) If any Student could not be present for PRC-II at the scheduled time (after approval and registration of his Project Work at PRC-I), his submission and presentation at the PRC-III time (or at any other PRC specified dates) may be treated as PRC-II performance evaluation, and delayed PRC-III dates for him may be considered as per PRC recommendations. Any Student is allowed to submit his M.Tech. Project Dissertation 'only after completion of 40 weeks from the date of approval/registration' of his Project, and after obtaining all approvals from the PRC.

d) A total of 200 Marks are allotted for the M.Tech. Project Work, (out of which 100 Marks are allotted for internal evaluation and 100 Marks for external evaluation). For internal Evaluation of 100 marks, Project Supervisor shall evaluate for 60 marks based on the continuous Internal Evaluation(CIE) of the student's performance and combined PRC-I, II & III performance evaluation will be for 40 marks (to be awarded by PRC, as SEE).

8.7 a) The Student shall be allowed to submit his Project Dissertation, only on the successful completion of all the prescribed PG Subjects (Theory and Labs.), Seminar, Comprehensive Viva-voce etc. (securing B Grade or above), and after obtaining all approvals from PRC. In such cases, the M.Tech. Dissertations will be sent to an External Examiner nominated by the Principal of the College, on whose 'approval', the Student can appear for the M.Tech. Project Viva-voce Examination, which shall be conducted by a Board, consisting of the PG Project Supervisor, Head of the Department, and the External Examiner who adjudicated the M.Tech. Project Work and Dissertation. The Board shall jointly declare the Project Work Performance as 'satisfactory', or 'unsatisfactory'; and in successful cases, the External Examiner shall evaluate the Student's Project Work presentation and performance for 100 Marks (SEE).

b) If the adjudication report of the External Examiner is 'not favourable' , then the Student shall revise and resubmit his Dissertation after one Semester, or as per the time specified by the External Examiner and/ or the PRC. If the resubmitted report is again evaluated by the External Examiner as 'not favourable', then that Dissertation will be summarily rejected. Subsequent actions for such Dissertations may be considered, only on the specific recommendations of the External Examiner and/ or PRC.

c) In cases, where the Board declared the Project Work Performance as 'unsatisfactory', the Student is deemed to have failed in the Project Vivavoce Examination, and he has to reappear for the Viva-voce Examination as per the Board recommendations. If he fails in the second Viva-

voce Examination also, he will not be considered eligible for the Award of the Degree, unless he is asked to revise and resubmit his Project Work by the Board within a specified time period (within 4 years from the date of commencement of his I Year I Semester).

9.0 Re-Admission / Re-Registration:

9.1 Re-Admission for Discontinued Students:

Students, who have discontinued the M.Tech. Degree Programme due to any reasons what so ever, may be considered for 'Readmission' into the same Degree Programme (with same specialization) with the Academic Regulations of the Batch into which he gets readmitted, with prior permission from the concerned authorities, subject to Item 4.1.

9.2 Re-Registration for Detained Students:

When any Student is detained in a Subject (s)/ Seminar due to shortage of attendance in any Semester, he may be permitted to re-register for the same Subject in the 'same category' (Core or Elective Group) or equivalent Subject if the same Subject is not available, as suggested by the Board of Studies of that Department, as when offered in the sub-sequent Semester(s), with the Academic Regulations of the Batch into which he seeks re-registration , with prior permission from the concerned authorities, subject to Item 4.1.

10.0 Grading Procedure:

10.1 Marks will be awarded to indicate the performance of each student in each Theory Subject, or Lab/Practicals, or Seminar, or Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item 6 above, and a corresponding Letter Grade shall be given.

10.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	*Letter Grade (UGC Guidelines)*	*Grade Points*
80% and above (≥ 80% , ≤ 100%)	O (Outstanding)	10
Below 80% but not less than 70% (≥ 70% , < 80%)	A^+ (Excellent)	9
Below 70% but not less than 60% (≥ 60% , < 70%)	A (Very Good)	8
Below 60% but not less than 55% (≥ 55% , < 60%)	B^+ (Good)	7
Below 55% but not less than 50% (≥ 50% , < 55%)	B (above Average)	6
Below 50% (< 50%)	F (FAIL)	0
Absent	**Ab**	**0**

10.3 A student obtaining F Grade in any Subject shall be considered 'failed' and is be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIEMarks) in those Subjects will remain the same as those he obtained earlier.

10.4 A Letter Grade does not imply any specific % of Marks.

10.5 A student earns Grade Point (GP) in each Subject/ Course, on the basis of the Letter Grade obtained by him in that Subject/ Course (excluding Mandatory non-credit Courses). Then the corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject/ Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

10.6 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (ΣCP) secured from ALL Subjects/ Courses registered in a Semester,
by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

$$\text{SGPA} = \{ \sum_{i=1}^{N} C_i \, G_i \} / \{ \sum_{i=1}^{N} C_i \} \ \ldots \ \text{For each Semester,}$$

where 'i' is the Subject indicator index (takes into account all Subjects in a Semester), 'N' is the no. of Subjects 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), is the no. of Credits allotted to the ith Subject, and represents the Grade Points (GP) corresponding to the Letter Grade awarded for that ith Subject.

10.7 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters.

CGPA is rounded off to TWO Decimal Places. CGPA is thus computed from the I Year second Semester onwards, at the end of each Semester, as per the formula

$$\text{CGPA} = \{ \sum_{j=1}^{M} C_j \, G_j \} / \{ \sum_{j=1}^{M} C_j \} \ \ldots \ \text{for all S Semesters registered}$$

(ie., upto and inclusive of S Semesters, S ≥ 1),

where ‘M’ is the TOTAL no. of Subjects (as specifically required and listed under the Course Structure of the parent Department) the Student has ‘REGISTERED’ from the 1st Semester onwards upto and inclusive of the Semester S (obviously M > N), ‘j’ is the Subject indicator index (takes into account all Subjects from 1 to S Semesters), is the no. of Credits allotted to the jth Subject, and represents the Grade Points (GP) corresponding to the Letter Grade awarded for that jth Subject. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

10.8 For Merit Ranking or Comparison Purposes or any other listing, ONLY the ‘ROUNDED OFF’ values of the CGPAs will be used.

10.9 For Calculations listed in Item 10.5 – 10.8, performance in failed Subjects/ Courses (securing F Grade) will also be taken into account, and the Credits of such Subjects/Courses will also be included in the multiplications and summations. However, Mandatory Courses will not be taken into consideration.

10.10 A student shall be declared successful or ‘passed’ in a Semester, only when he gets a SGPA ≥ 5.00 (at the end of that particular Semester); and a student shall be declared successful or ‘passed’ in the entire M. TECH, only when gets a CGPA ≥ 5.00; subject to the condition that he secures a GP ≥ 6 (B Grade or above) in every registered Subject/ Course in each Semester (during the entire M. TECH) for the Degree Award, as required.

10.11 After the completion of each Semester, a Grade Card or Grade Sheet (or Transcript) shall be issued to all the Registered Students of that Semester, indicating the Letter Grades and Credits earned. It will show the details of the Courses Registered (Course Code, Title, No. of Credits, Grade Earned etc.), Credits earned, SGPA, and CGPA.

10.12 Passing Standards :

10.12.1 A Student shall be declared successful or ‘passed’ in a Semester, only when he gets a SGPA ≥ 5.00 (at the end of that particular Semester); and a Student shall be declared successful or ‘passed’ in the entire M. TECH, only when gets a CGPA ≥ 5.00; subject to the condition that he secures a GP ≥ 6 (B Grade or above) in every registered Subject/ Course in each Semester (during the entire M. TECH), for the Award of the Degree, as required.

10.12.2 After the completion of each Semester, a Grade Card or Grade Sheet (or Transcript) shall be issued to all the Registered Students of that Semester, indicating the Letter Grades and Credits

earned. It will show the details of the Courses Registered (Course Code, Title, No. Of Credits, Grade Earned), Credits earned, SGPA, and CGPA etc.

11.0 Declaration of Results:

11.1 Computation of SGPA and CGPA are done using the procedure listed in 10.5 – 10.8.

11.2 For Final % of Marks equivalent to the computed CGPA, the following formula may be used ..

% of Marks = (CGPA – 0.5) x 10

12.0 Award of Degree and Class:

12.1 A Student who registers for all the specified Subjects/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (M. TECH), and secures the required number of **90** Credits (with GP ≥ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

12.2 Award of Class

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following four classes based on the % CGPA:

Class Awarded	CGPA
First Class with Distinction	≥ 7.75
First Class	6.75 ≤ CGPA < 7.75
Second Class	5.75 ≤ CGPA < 6.75
Pass Class	5.0 ≤ CGPA < 5.75

12.3 A student with final CGPA (at the end of the M. TECH) < 5.00 will not be eligible for the Award of Degree.

13.0 Withholding of Results:

13.1 If a Student has not paid fees to University/ College at any stage, or has pending dues

against his name due to any reason whatsoever, or if any case of indiscipline is pending against him, the result of the Student may be withheld, and he will not be allowed to go into the next higher Semester.

The Award or issue of the Degree may also be withheld in such cases.

14.0 Transitory Regulations:

14.1 A Student - who has discontinued for any reason, or who has been detained for want of attendance as specified, or who has failed after having undergone M. TECH, may be considered eligible for readmission to the same M. TECH with same set of Subjects/ Courses (or equivalent Subjects/ Courses as the case may be), and same Professional Electives (or from same set/category of Electives or equivalents as suggested), as and when they are offered (within the timeframe of 4 years from the Date of Commencement of his I Year I Semester).

15.0 Student Transfers:

15.1 There shall be no Branch/ Specialization transfers after the completion of Admission Process.

16.0 Scope:

i) Where the words "he", "him", "his", occur in the write-up of regulations, they include "she", "her", "hers".

ii) Where the words "Subject" or "Subjects", occur in these regulations, they also imply "Course" or "Courses".

iii) The Academic Regulations should be read as a whole, for the purpose of any interpretation.

iv) In case of any doubt or ambiguity in the interpretation of the above regulations, the decision of the Vice-Chancellor/ Principal is final.

v) The College may change or amend the Academic Regulations, and/ or Course Structure, and/ or Syllabi at any time, and the changes or amendments made shall be applicable to all Students with effect from the dates as notified by the University/ College.

	Nature of Malpractices If the candidate:	**Punishmen t**
1 (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other formof material concerned with orrelated to the subject of the	Expulsion from the examination hall and cancellation of the performance in thatsubject only.

	examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	
1 (b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examinationhall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/year. The Hall Ticket of the candidate is to becancelled.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connectionwith forfeiture of seat. If the

		imposter is an outsider, he will be handed over to the police and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjectsof that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him toaward pass marks.	Cancellation of the performance in thatsubject.
6	Refuses to obey the orders of the Chief Superintendent / Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

	relations, or indulges in any otheract of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination	
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjectsof that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connectionwith forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjectsof that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and allother subjects the candidate has

	person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	already appeared including practical examinations and project work and shallnot be permitted for the remainingexaminations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further Action to award suitable punishment.	

18. GENERAL:

• **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

• **Credit Point:** It is the product of grade point and number of credits for a course.

• The Academic Regulations should be read as a whole for the purpose of any interpretation.

• The University/College reserves the right of altering the Academic Regulations and/or Syllabus/Course Structure, as and when necessary. The modifications or amendments may be applicable to all the candidates on rolls, as specified by the University/College.
• Wherever the words ‘he’ or ‘him’ or ‘his’ occur in the above regulations, they will also include ‘she’ or ‘her’ or ‘hers’.
• Wherever the word ‘Subject’ occurs in the above regulations, it implies the ‘Theory Subject’, ‘Practical Subject’ or ‘Lab.’ and ‘Seminar’.
• In case of any ambiguity or doubt in the interpretations of the above regulations, the decision of the Principal shall be final.

******

M.Tech (VLSI SYSTEM DESIGN)

I YEAR -I SEMESTER

Course Code	Course	L	T/P/D	Evaluation			Credits
				CIE	SEE	TOT	
16MVS101	CMOS Analog Integrated Circuit Design	**4**	**-**	**30**	**70**	**100**	**4**
16MVS102	CMOS Digital Integrated Circuit Design	**4**	**-**	**30**	**70**	**100**	**4**
	Elective - I	**4**	**-**	**30**	**70**	**100**	**4**
16MVS103	Digital System Design						
16MVS104	Hardware Software Co-design						
16MVS105	Advanced Digital Design Through Verilog						
	Elective – II	**4**	**-**	**30**	**70**	**100**	**4**
16MVS106	VLSI Design Automation						
16MVS107	Embedded System Design						
16MVS108	Advanced operating Systems						
	Elective – III	**4**	**-**	**30**	**70**	**100**	**4**
16MVS109	Device Modeling						
16MVS110	Nano Electronics / Technology						
16MVS111	VLSI Technology						
	Elective – IV	**4**	**-**	**30**	**70**	**100**	4
16MVS112	PLD Architecture and Applications						
16MVS113	Advanced Data Communication						
16MVS114	Advanced Digital Signal Processing						
	SEMINAR/ LAB						
16MVS1S1	Seminar	**-**	**4**	**100**	**-**	**100**	**2**
16MVS1L1	VLSI Lab – I	**-**	**4**	**30**	**70**	**100**	**2**
	Total	**24**	**8**	**310**	**490**	**800**	**28**

I YEAR - II SEMESTER

Course Code	Course	L	T/P/D	Evaluation			Credits
				CIE	SEE	TOT	
16MVS201	Design for Testability	**4**	**-**	**30**	**70**	**100**	**4**
16MVS202	Mixed Signal Circuit Design	**4**	**-**	**30**	**70**	**100**	**4**
	Elective – V	**4**	**-**	**30**	**70**	**100**	**4**
16MVS203	VLSI and DSP Architectures						
16MVS204	Custom IC Design						
16MVS205	VLSI Interconnects and Design Techniques						
	Elective – VI	**4**	**-**	**30**	**70**	**100**	**4**
16MVS206	Optimization Techniques in VLSI Design						
16MVS207	System on Chip Architecture						
16MVS208	Semiconductor Memory Design and Testing						
	Elective – VII	**4**	**-**	**30**	**70**	**100**	**4**
16MVS209	Low power VLSI Design						
16MVS210	Digital HDL Design and Verification						
16MVS211	High Speed VLSI						
	Elective - VIII	**4**	**-**	**30**	**70**	**100**	**4**
16MVS212	Scripting Languages						
16MVS213	VLSI Signal Processing						
16MVS214	Advanced Computer Architecture						
	LABORATORIES/SEMINARS						
16MVS2L1	VLSI Laboratory - II	**-**	**4**	**30**	**70**	**100**	2
16MVS2S1	Soft Skills	**-**	**4**	**100**	**-**	**100**	**2**
	Total	**24**	**8**	**310**	**490**	**800**	**28**

II Year –I Semester								
Course Code	**Course**	**L**	**T**	**P**	**Evaluation**			**Credits**
					CIE	**SEE**	**TOT**	
16MVS3C1	Comprehensive Viva-Voce	**-**	**-**	**-**	**-**	**100**	**-**	**4**
16MVS3P1	Project Phase –I	**-**	**-**	**-**	**-**	**-**	**-**	**12***
						Total Credits		**16**

II Year –II Semester								
Course Code	**Course**	**L**	**T**	**P**	**Evaluation**			**Credits**
					CIE	**SEE**	**TOT**	
16MVS4P1	Project Phase-II & Dissertation	**-**	**-**	**-**	**100**	**100**	**200**	**18***
						Total credits		**18**

*Credits will be awarded only at the end of Semester End Examination (SEE). Marks Memo for project shall be generated only after successful completion of the project.

Academic Year 2016-17

16MVS101 - CMOS ANALOG INTEGRATED CIRCUIT DESIGN

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. EDC
2. ECA
3. VLSI Design

Course Objectives:

1. To impart knowledge about MOS devices, passive components, Layout making and modeling of CMOS ICs (both small signal and large signal).
2. To provide insight into analog CMOS sub circuits like switch, diode, current sinks, current sources, current mirrors, voltage references, band gap references etc..
3. To provide knowledge of CMOS Amplifiers like Inverters, Differential amplifiers, High gain amplifiers, Cascade amplifiers etc.
4. To provide insight into CMOS operational Amplifiers and measurement of various parameters like Gain, CMRR, PSRR etc
5. To provide basic understanding of comparators with emphasis on Open loop comparators, two stage comparators, Discrete time comparators.

Course Outcomes: At the end of this course the students will be able to

1. Model the MOS & CMOS devices for small signal as well as large signal and will be able to make layouts.
2. Explain the functioning of Analog MOS , sub units like MOS switch , MOS active resistor, Current sources , Current mirrors etc.
3. Explain the working of CMOS amplifiers like Inverters, Differential amplifiers, Current amplifiers, High gain amplifiers.
4. Distinguish the functioning of CMOS Operational Amplifiers, Cascode Amplifiers with emphasis on measurement of various parameters like Gain, CMRR, PSRR etc.
5. Explain the working of comparators of different types like Single stage, two stage, open loop and Discrete time comparators

UNIT -I: MOS Devices Modeling: The MOS Transistor, Passive Components- Capacitor & Resistor, and Integrated circuit Layout.

UNIT -II Modelling: CMOS Device Modelling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -III: Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -IV CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -V CMOS Operational Amplifiers and Comparators: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp. **Comparators:** Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Text Books:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

Reference Books:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

Academic Year 2016-17

16MVS102 - CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. STLD
2. VLSI Design

Course Objectives:

1. To impart knowledge on MOS design with emphasis on MOS inverters MOS output voltage, gain transient response rise time etc.
2. To develop equivalent models of MOS/CMOS gates.
3. To impart Knowledge on combinational MOS logic circuits like NMOS and PMOS gates, realization of complex Boolean expressions using NMOS gates and CMOS gates.
4. Providing insight into the working of Transmission gates, AND-OR-INVERT gates, OR-AND-INVERT gates and realization of complex Boolean expressions using these gates.
5. To provide insight into sequential MOS logic circuits like Latches, D Flip Flops, JK Flip flops.
6. To make the students understand the working of dynamic logic circuits of CMOS.
7. To import knowledge in semiconductor memories like Dynamic memories, Static memories, NAND / NOR flash memories.

Course outcomes: At the end of the course the students will be able to:

1. Explain the functioning of Pseudo NMOS inverter its gain, output logic voltages, Transient response, Rise time, Fall time.
2. Develop equivalent modes of NMOS and CMOS gates.
3. Distinguish MOS logic gates like NAND&NOR and also able to design complex Boolean expressions using them.
4. Explain transmission gates, AND OR INVERT gates, OR AND INVERT gates and realization of complex Boolean expressions using these gates.
5. Distinguish the working of sequential MOS logic circuits like latches, D Flip Flops, JK Flip Flops.
6. Explain the working of dynamic logic circuits using CMOS, working of Memories using CMOS ICs, static memories, dynamic memories NAND NOR Flash Memories.

UNIT –I: MOS Design: Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage.

UNIT –II: Timing Analysis: Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –III: Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –IV: Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT –V: Dynamic Logic Circuits and **Semiconductor Memories:** Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits. **Semiconductor Memories** :Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

Text Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

Academic Year 2016-17

16MVS103 - DIGITAL SYSTEM DESIGN
(Elective –I)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. STLD
2. VLSI Design

Course Objectives:

1. To Provide a comprehensive understanding of the principles and practices of digital logic circuits
2. To make the Students should be able to analyze, design and implement combinational and sequential circuits.
3. The laboratory sessions form an integral part to provide practical experiences in hardware and software analysis and design.
4. To understand the basic FSM design and also reduction of flow table and state table
5. To understand the basic concepts of testing VLSI circuits.
6. To draw State Machine charts.

Course Outcomes: At the end of the course the students will be able to:

1. Describe, design, simulate, and synthesize computer hardware using the Verilog HDL
2. Design combinational and sequential logic circuits.
3. Design complex state machines (present in all practical computers).
4. Synthesize logic and state machines using an Automatic Logic Synthesis program. Implement state machines using Field-Programmable Gate Arrays.
5. Design high-speed computer arithmetic circuits. Design a computer memory using error-correcting codes.
6. Design a self test facility for a computer system.
7. Explain Fault Tolerance to be provided in a computer system.

UNIT -I: Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II: Digital Design: Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, array multiplier, Keypad Scanner, Binary divider.

UNIT -III: SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV: Fault Modeling & Test Pattern Generation: Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

UNIT-V: Fault diagnosis of combinational circuits and Fault Diagnosis in Sequential Circuits: Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults. **Fault Diagnosis in Sequential Circuits:** Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Text Books:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH

Reference Books:

1. Logic Design Theory – N. N. Biswas, PHI
2. Digital Circuits and Logic Design – Samuel C. Lee , PHI
3. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.

Academic Year 2016-17

16MVS104 - HARDWARE - SOFTWARE CO-DESIGN
(Elective- I)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. Advanced Computer Architecture
2. Embedded Systems

Course Objective:

1. To provide a broad understanding of the specific requirement of Hardware and soft ware integration for embedded system

Course Outcomes:

1. To acquire the knowledge on various models.
2. To explore the interrelationship between Hardware and software in a embedded system.
3. Acquire the knowledge of firmware development process and tools.
4. Understand validation methods and adaptability.

UNIT –I: Co- Design and Co- Synthesis:
Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. **Co- Synthesis Algorithms:** Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II: Prototyping, Emulation and Target Architectures:
Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure. **Target Architectures:** Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III: Compilation Techniques and Tools:
Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV: Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIY – V: Languages for System – Level Specification and Design:
Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages.

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Text Books:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

Reference Books:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer.
2. Embedded System Design: A Unified Hardware/Software Approach ‰ Frank Vahid and Tony Givargis, 1999.

Academic Year 2016-17

16MVS105 - ADVANCED DIGITAL DESIGN THROUGH VERILOG
(Elective- I)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. STLD
2. DDVH

Course Objectives:

1. To provide knowledge on hardware modelling descriptive styles and design methodologies.
2. To provide knowledge on data types and operators for modelling of delays in Verilog.
3. To provide knowledge on behavioural modelling in Verilog using different assignments of blocking and non-blocking.
4. To provide knowledge on synthesis of combinational logic.
5. To provide knowledge on synthesis of sequential logics
6. To provide basics of Verilog constructs and conventions along with synthesis process.

Course Outcomes: Upon successful completion of the course, students will be able to:

1. Explain the hardware modelling Verilog primitives and descriptive styles and representation of numbers.
2. Explain data types and operators for modelling in verilog and models of propagation delays.
3. Analyze behavioural descriptions in verilog like assignment of blocking and non-blocking and delays and constructs in verilog.
4. Interpret synthesis of combinational logics and registers.
5. Interpret synthesis of counters and finite state machines.
6. Interpret the synthesis of language constructs like nets, operators, registers and user defined primitives and Timings Controls in Synthesis.

UNIT I: Hardware Modeling With The Verilog HDL : Hardware Encapsulation –The Verilog Module, Hardware Modelling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioural Description In Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

UNIT II: Logic System, Data Types And Operators For Modeling In Verilog HDL: User-Defined Primitives, User Defined Primitives – Combinational Behaviour User-Defined Primitives –Sequential Behaviour, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions and Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT III: Behavioral Descriptions In Verilog HDL: Verilog Behaviour, Behavioural Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioural Models of Finite State Machines.

UNIT IV: Synthesis Of Combinational Logic: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Three State Outputs and Don't Cares.

UNIT V: Synthesis Of Sequential Logic: Synthesis of Sequential UDPs, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines, Resets, Synthesis of Gated Clocks, Design Partitions and Hierarchical Structures. **Synthesis Of Language Constructs:** Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

Text Books:

1. M.D.CILETTI, "Modelling, Synthesis and Rapid Prototyping with the Verilog HDL", Prentice-Hall, 1999.
2. Z.NAWABI, "VHDL Analysis and Modelling of Digital Systems", (2/E), McGraw Hill, 1998.

Reference Books:

1. M.G.Arnold, "Verilog Digital – Computer Design", Prentice-Hall (PTR), 1999.
2. Perry, "VHDL", (3/E), McGraw Hill.

Academic Year 2016-17

16MVS106 - VLSI DESIGN AUTOMATION

(Elective- II)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. VLSI Design

Course objectives:

1. To provide knowledge on VLSI design methodologies design flows and design automation tools
2. To provide knowledge on various optimization techniques in the process of automation.
3. To provide ability of designing logic using different modeling schemes.
4. To provide knowledge on different types of logic synthesis and simulation for designing VLSI circuits
5. To provide knowledge on FPGA physical design partitioning, floor-planning, placement and routing
6. To provide knowledge on MCMS physical design partitioning, floor-planning, placement and Different types of routing techniques

Course Outcomes: After completion of the course students are able to

1. Model automation of VLSI design
2. Apply optimization techniques to the process of VLSI design.
3. Design logic in data flow, structural and behavioral modeling.
4. Design field programmable gate array using different kinds of methodologies.
5. Design MCMS physical design using automation tools.
6. Synthesize and verify the output of VLSI Circuits.

UNIT I: Preliminaries : Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II: General Purpose Methods For Combinational Optimization: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III: Layout Compaction, Placement, Floor planning And Routing: Problems, Concepts and Algorithms. Modeling And Simulation Gate Level Modeling and Simulation, Switch level modeling and Simulation.

UNIT IV: Logic Synthesis And Verification : Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis High-Level Synthesis Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V: Physical Design Automation Of FPGAs : FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models. **Physical Design Automation Of MCMs :** MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple

stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

Text Books:

1. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John Wiley & Sons (Asia) Pvt. Ltd.
2. Algorithms for VLSI Physical Design Automation Naveed Sherwani, 3rd Ed., 2005, Springer International Edition.

Reference Books:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia.

Academic Year 2016-17

16MVS107 - EMBEDDED SYSTEMS DESIGN

(Elective- II)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Prerequisite: Microprocessor and Microcontrollers

Course Objectives:

1. To provide an overview of Design Principles of Embedded System.
2. To provide clear understanding about the role of firmware, operating systems in correlation with hardware systems.

Course Outcomes:

1. Expected to understand the selection procedure of Processors in the Embedded domain.
2. Design Procedure for Embedded Firmware.
3. Expected to visualize the role of Real time Operating Systems in Embedded Systems.
4. Expected to evaluate the Correlation between task synchronization and latency issues

UNIT -I: Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II: Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS),

UNIT -III: Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -IV: Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -V: RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling. **Task Communication:** Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

Text Books:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.
2. Embedded Systems - Raj Kamal, TMH.

Reference Books:

1. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
2. Embedded Systems – Lyla, Pearson, 2013
3. An Embedded Software Primer - David E. Simon, Pearson Education.

Academic Year 2016-17

16MVS108 - ADVANCED OPERATING SYSTEMS

(Elective- II)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s): Computer Organization and Operating Systems

Course Objectives:

1. To explain the basics of operating systems and its history.
2. To introduce the main features of Unix/Linux operating system.
3. To explain the Unix/Linux OS internals and mechanism of various inter process communication policies.
4. To explain the issues in Distributed Systems and various policies of achieving synchronization in Distributed systems

Course Outcomes: At the end of the course, a student will be able to:

1. Demonstrate and compare various Operating Systems based on their features.
2. Gain the knowledge to understand the Unix/Linux OS and can customize according to the requirements.
3. Gain knowledge in writing software routines, modules or patches for the operating systems, using respective system calls.
4. Implement modules achieving Inter Process Communication (IPC) through various mechanisms and analyzing their performance.
5. Explain the requirements of Distributed Systems and can solve the challenges in setting up the distributed systems.

UNIT –I: Introduction to Operating Systems: Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication Techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II: Introduction to UNIX and LINUX: Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT –III: System Calls: System calls and related file structures, Input / Output, Process creation & termination. **Inter Process Communication:** Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV: Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues. **Communication in Distributed Systems:** Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V: Synchronization in Distributed Systems: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions. **Deadlocks:** Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

Text Books:

1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.

Reference Books:

1. The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.
2. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
3. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
4. Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley.
5. UNIX User Guide – Ritchie & Yates.
6. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

Academic Year 2016-17

16MVS109 - DEVICE MODELLING
(Elective -III)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. **Electronic Devices and Circuits**
2. **VLSI Design**

Course Objectives:

1. To provide knowledge of principles of semiconductor devices for integrated circuits.
2. To provide basic understanding of fundamental concepts in semiconductor physics including Quantum Mechanics, Boltzmann transport, continuity and poisons equations.
3. To provide insight into monolithic technology and model parameters to develop integrated passive devices such as capacitors and resistors.
4. To provide basic understanding of modeling aspects of integrated diodes and BJTsin monolithic technologies and spice models.
5. To impart knowledge of integrated MOSFET (NMOS and PMOS) and it realization through MOS FET SPICE model level 1, 2, 3 and 4.
6. To provide an overview of VLSI fabrication techniques involved in development of integrated circuits of MOS technology.
7. To provide knowledge on modeling aspects of Hetero Junction Devices.

Course Outcomes: At the end of this course student will be able to

1. Explain the principles of Quantum Mechanics, Boltzmann transport, continuity and poisons equations and their application to integrated semiconductor devices.
2. Describe monolithic technologies for development of passive integrated devices.
3. Develop basic understanding of integrated diodes and BJTs in monolithic technologies, and also can analyze the SPICE models.
4. Analyze the DC/AC characteristics and basic equations of MOS device and can also develop models of field effect devices.
5. Categorize the processing steps involved in VLSI fabrication of semiconductor devices.

UNIT -I: Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

UNIT -II: Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures.

UNIT -III: Integrated Diodes: Junction and Schottky diodes in monolithic technologies– Static and Dynamic behavior – Small and large signal models – SPICE models. **Integrated Bipolar Transistor:** Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model-dynamic model, Parasitic effects – SPICE model –Parameter extraction.

UNIT -IV: Integrated MOS Transistor: NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics– MOS FET SPICE model level 1, 2, 3 and 4.

UNIT -V: VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate NMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements. **Modelling of Hetero Junction Devices:** Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe.

Text Books:

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.

Reference Books:

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.

Academic Year 2016-17

16MVS110 - NANO ELECTRONICS/TECHNOLOGY
(Elective -III)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. Electronic Devices and Circuits
2. VLSI Design

Course objectives

1. To provide knowledge on drawbacks of MOSFET in comparison with other FETS and NANO tubes
2. To provide knowledge on basic of single electron transistors and resonant tunneling Diodes
3. To provide knowledge on various carbon NANO tubes and its applications
4. To provide knowledge on coherent and incoherent transport of electrons
5. To provide knowledge on spin devices logic device and microwave oscillators
6. To provide ability of differentiating spin and charge electrons concepts and their advantages.

Course outcomes:

1. Able to Explain the operation of MOSFET, SOI MOSFET and fin FET and analyze their drawbacks
2. Able to distinguish the operation of single electron devices and resonant tunneling diodes.
3. Able to Distinguish NANO tubes and MOSFETS and understand their applications.
4. Able to analyze the operation of molecular electron and evaluate for coherent and incoherent transport of it.
5. Able to categorize the spin electron and applications of spin electrons.
6. Able to compare the charge electron and applications of spin electrons.

UNIT I - Limitation Of MOSFETs: Classical mechanics and its drawbacks, Quantum mechanics, 1D problem - particle in a box, electron tunnelling., MOSFET scaling, Non-uniform doping in channel, high K dielectrics, SOI MOSFET, Buried channel MOSFET, Fin FET.

UNIT II - Single Electronics: Coulomb blockade, Electron tunnelling devices, Single electron transistors, Resonant Tunnelling Diodes.

UNIT III- Carbon Nano Tubes: Carbon Nano tubes – Basic structures, CNTFETs, Applications.

UNIT IV - Molecular Electronics: Molecular wire conductance - Theories of Coherent Electron Transport in molecular junctions, Evaluation of the conductance for coherent transport, Incoherent transport and vibronic coupling, Molecular circuit elements, Circuits.

UNIT V – Spintronics: Spin Vs charge, AMR, GMR, TMR, Spin devices- Spin valves, Magnetic tunnel junctions. **Applications QCA & Memories:** Principle and applications, Quantum computing, Quantum cellular automata. Applications – memories (MRAM, STRAM), Logic device, and microwave oscillators.

Text Books:

1. Chonles P.Poole Jr., Frank. J. Owens, *"Introduction to NanoTechnology",* John Wiley and Sons, 2009.
2. Phani Kumar, "Principles of Nano-Technology", Scitech publications, 2nd edition, 2010.

Reference Books:

1. Rainer Waser, *"Nano Electronics and Information Technology:Advanced Electronic Materials and Novel Devices"*, 2nd Edition,Wiley-VCH, 2012.
2. T. Pradeep, *"Nano: The essentials",* Tata McGraw Hill, 2007.
3. Mark A. Ratner, Danill Ratner, *"Nano Technology: A Gentle Introduction to the Next Big Idea",* Prentice Hall, 2003.

Academic Year 2016-17

16MVS111 - VLSI TECHNOLOGY
(Elective -III)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s): Electronic Devices and Circuits

Course Objectives:

1. To provide an insight in to the different MOS and CMOS technologies.
2. To provide knowledge in various design tools for layout of MOS circuits.
3. To provide a overview of different stages of semiconductor devices manufacturing like wafer fabrication, oxidation, photolithography, photo masking etc,.
4. To provide insight in to basic concepts about doping of semiconductors materials, diffusion process, ion implantation etc,.
5. To impart basic concepts about design rules of MOS, BICMOS ICs including packaging operations.

Course Outcomes: At the end of the course students will be able to

1. Explain the different MOS, CMOS, BiCMOS technologies with the associated electrical properties and problems like Latch up.
2. Develop the equivalent circuit models, current and voltage relationships in MOS & CMOS ICs.
3. Distinguish layout design tools for different logic gates including interconnect delays associated with the layouts.
4. Categorize the manufacturing stages involved in semi conductor industry like crystal growth, basic wafer fabrication process yields, oxidation, photolithography doping, Depositions, Metallization, photo masking etc,.
5. Explain the process of doping, depositions, diffusion, ion implantation epitoxy etc, used in semi conductor industry.
6. State design rules of MOS/BICMOS ICs including packaging operations.

UNIT –I: Review Of Microelectronics And Introduction To Mos Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II: Layout Design And Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III: Overview Of Semiconductor Industry: Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction.

UNIT –IV: IC Fabrication Process: Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT –V: Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitoxy, molecular beam epitaxy. Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors, Packaging: Chip characteristics, package functions, package operations.

Text Books:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994

Reference Books:

1. Micro Electronics circuits Analysis and Design 2nd Edition, Muhammad H Rashid, CENAGE Learning2011.
2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999
3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000
4. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
5. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

Academic Year 2016-17

16MVS112 - PLD ARCHITECTURE AND APPLICATIONS
(Elective -IV)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. STLD
2. VLSI Design

Course Objectives:

1. To understand the basic concept of Programmable Logic Devices and the function of various complex Programmable Logic Devices.
2. To acquire knowledge on FPGAs programming technologies and applications.
3. To get the command over different Xilinx architectures.
4. To gain the knowledge on various ACTEL Architectures.
5. To implement various applications using FPGAs.

Course Outcomes: After completion of the course students are able to

1. Explain the function of basic PLDs and CPLDs.
2. Explain the organization of FPGAs and its applications.
3. Describe programming technology of SRAM programmable FPGAs and various Xilinx architectures.
4. Describe the programming technology of Anti-Fuse programmed FPGAs and different Actel architectures.
5. Explain how the FPGAs are used to implement various real time applications.

UNIT-I: Introduction to Programmable Logic Devices (PLD): Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic.

UNIT-II: Complex Programmable Logic Devices: Introduction –Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-III: Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT –IV: SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -V: Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, the Actel ACT1, ACT2 and ACT3Architectures. **Design Applications:** General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot

Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

Reference Books:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Field Programmable Gate Arrays – Stephen D.Brown,Robert, J. Francis Springer International Edition.
3. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
4. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
5. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

Academic Year 2016-17

16MVS113 - ADVANCED DATA COMMUNICATIONS
(Elective -IV)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. Digital Communications
2. Computer Networks

Course Objectives:

1. To learn about basics of Data Communication networks, different protocols, standards and layering concepts.
2. To study about error detection and correction techniques.
3. Know about link layer protocol and point to point protocols.
4. To understand Medium Access Control sub layer protocols
5. To know about Switching circuits, Multiplexing and Spectrum Spreading techniques for data transmission.
6. To study Wired LANs different Ethernet standards

Course Outcomes: At the end of the course, the student will be able to:

1. Understand the concepts of Data Communication networks, different protocols, standards and layering.
2. Acquire the knowledge of error detection, forward and reverse error correction techniques.
3. Analyze link layer protocol and point to point protocols
4. Explain and compare the performance of different MAC protocols like Aloha, CSMA, CSMA/CA, TDMA, FDMA & CDMA.
5. Understand the features and the significance of Switching circuits, Multiplexing and Spectrum Spreading for data transmission .
6. Understand the characteristics of Wired LANs and also the operation and applications of Connecting Devices
7. Understand the services and functions of Network layer protocols.

Unit I: Data Communications and Layered Structures: Data Communications, Networks and Network Types, Internet History, Standards and Administration, Protocol Layering, TCP/IP protocol suite, OSI Model. Digital Data Transmission, DTE-DCE interface. **Data Link Layer:** Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol.

Unit II: Error Detection and Correction: Types of Errors, Redundancy, detection versus correction, Coding Block Coding: Error Detection, Vertical redundancy cheeks, longitudinal redundancy cheeks, Error Correction, Error correction single bit, Hamming code. **Cyclic Codes**: Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum. **Data Link Control**: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol.

Unit III: Media Access Control (MAC) Sub Layer: Random Access, Aloha, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation, Polling-Token Passing, Channelization - Frequency Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA).

Unit IV: Switching: Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of switch. **Multiplexing and Spectrum Spreading:** Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing, Spread Spectrum -Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum.

Unit V: Wired LANS: Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Giga bit Ethernet. **Connecting Devices:** Hubs, Link Layer Switches, Routers. **Networks Layer:** Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic Host Configuration Protocol (DHCP), Network Address Resolution(NATF), Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches.

Text Books:

1. Data Communications and Networking - B. A. Forouzan, 5th , 2013,TMH.
2. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.

Reference Books:

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data Communications and Computer Networks- Brijendra Singh, 2nd ed., 2005, PHI.

Academic Year 2016-17

16MVS114 - ADVANCED DIGITAL SIGNAL PROCESSING
(Elective -IV)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s): Digital Signal Processing

Course Objectives: The objectives of this course are to make the student

1. Understand the design of various types of digital filters and implement them using various implementation structures and study the advantages & disadvantages of a variety of design procedures and implementation structures.
2. Understand the concept and need for Multirate signal Processing and their applications in various fields of Communication & Signal Processing
3. Understand difference between estimation & Computation of Power spectrum and the need for Power Spectrum estimation.
4. Study various Parametric & Non parametric methods of Power spectrum estimation techniques and their advantages & disadvantages
5. Understand the effects of finite word/register length used in hardware in implementation of various filters and transforms using finite precision processors.

Course Outcomes: On completion of this course student will be able to

1. Design and implement a filter which is optimum for the given specifications.
2. Design a Mutirate system for the needed sampling rate and can implement the same using Polyphase filter structures of the needed order.
3. Estimate the power spectrum of signal corrupted by noise through a choice of estimation methods: Parametric or Non Parametric.
4. Can calculate the output Noise power of different filters due to various finite word length effects viz: ADC Quantization, product quantization, and can calculate the scaling factors needed to avoid Limit cycles: Zero input, overflow. Also they can decide the stability of the system by studying the effect due to coefficient quantization while implementing different filters and transforms.

UNIT –I: Review of DFT, FFT, IIR Filters and FIR Filters: Introduction to filter structures (IIR & FIR).Implementation of Digital Filters, specifically 2^{nd} Order Narrow Band Filter and 1^{st} Order All Pass Filter. Frequency sampling structures of FIR, Lattice structures, Forward prediction error, Backward prediction error, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT -II: Non-Parametric Methods: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman-Tukey methods, Comparison of all Non-Parametric methods.

UNIT - III: Parametric Methods: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation, Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

UNIT –IV: Multi Rate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion. Examples of up-sampling using an All Pass Filter.

UNIT –V: Applications of Multi Rate Signal Processing: Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Subband Coding of Speech Signals, Quadrature Mirror Filters, Transmultiplexers, Over Sampling A/D and D/A Conversion.

Text Books:

1. Digital Signal Processing: Principles, Algorithms & Applications - J.G.Proakis& D. G. Manolakis, 4th Ed., PHI.
2. DSP – A Practical Approach – Emmanuel C. Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

Reference Books:

1. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
2. Modern spectral Estimation: Theory & Application – S. M .Kay, 1988, PHI.
3. Multi Rate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education.
4. Digital Signal Processing: A Practitioner's Approach, Kaluri V. Rangarao, Ranjan K. Mallik ISBN: 978-0-470-01769-2, 210 pages, November 2006 John Weley.
5. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

Academic Year 2016-17

16MVS1L1 - VLSI Lab – I

I Year – I Sem M. Tech

L	T	P	C
-	-	4	2

Pre-requisite(s):

1. STLD
2. DDVH

Lab Objectives: Students will be able to

1. Understand, describe, simulate and synthesize combinational logic circuits using Verilog
2. Understand, describe, simulate and synthesize sequential logic circuits using Verilog
3. Analyze simulation results of a complex circuit and implement on FPGA trainer Board.
4. Implement an idea based on FSM (Mealy or Moore Machine) and describe using Verilog.

Lab Outcomes: Students will be able to

1. Design combinational and sequential logic circuits.
2. Develop HDL code using Verilog for combinational and sequential logic circuits.
3. Simulate and Synthesize the HDL Code using EDA Tools.
4. Interpret the simulation results for simple and complex circuits.
5. Develop code for an FSM based design (Mealy or Moore Machine) using Verilog.

VLSI Front End Design programs:

Programming can be done using any HDL Complier (Verilog HDL), Verification of the Functionality using Functional Simulator, Timing Simulation for Critical Path time Calculation, Synthesis, Place & Route and Implementation of Design using FPGA Boards / Trainer Kits.

List of Experiments: (Minimum 13 experiments are to be conducted)

1. Design of XOR gate using 2 input NAND gates
2. Design of 3-to-8 decoder using 2-to-4 decoder
3. Design of 8-to-3 encoder (without and with parity)
4. Design of 8-to-1 multiplexer and 1-to-8 demultiplexer
5. Design of 4 bit binary to gray converter
6. Design of 4 bit comparator
7. Design of Half and Full adders, Serial Binary Adder, Carry Look Ahead Adder.
8. Design of JK Flip Flop using DFF and also TFF
9. Design of a 4-bit Shift Register of Serial in Serial out, Serial in Parallel out, Parallel in Serial out and Parallel in Parallel Out
10. Design of 4-bit Binary, BCD Counters (Synchronous/ Asynchronous Reset)
11. Design of 4-bit Ring and Johnson Counters
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines)
13. Design of 4 Bit Multiplier
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Complement, Multiplication and Division.
15. Design of Vending Machine Controller.

Note:- All the above digital circuits are to be designed and implemented using Cadence /Mentor Graphics / Synopsys / Xilinx / Equivalent CAD tools.

Academic Year 2016-17

16MVS201 - DESIGN FOR TESTABILITY

L	T	P	C
4	-	-	4

I Year – I Sem M. Tech

Pre-requisite(s):

1. STLD
2. VLSI Design

Course Objectives:

1. To make students understand about philosophy and types of vlsi testing techniques.
2. To make students understand about different levels of testing fault models.
3. To make students understand how to develop logic and proceed for fault simulation
4. To make students understand about the advancements in testing measurements.
5. To make students understand about delay and pattern generations.
6. To import knowledge on different scan standards.

Course Outcomes: At the end of the course students will be able to:

1. Distinguish different VLSI based technology trends.
2. Explain defects and errors in fault modeling.
3. Explain test evaluation process and design verification in software.
4. Interpret high measure testing levels and variations of scan.
5. Explain economic case and delay faults of BIST.
6. Distinguish different pin constraints and configuration techniques.

UNIT -I: Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing,

UNIT -II: Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -III: Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -IV: Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -V: Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST. **Boundary Scan Standard:** Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Text Books:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.
2. Testing of Digital Systems, N K JHA and S GUPTA, Cambridge University Press, 2003.

Reference Books:

1. Testing of Digital Systems, N K JHA and S GUPTA, Cambridge University Press, 2003.
2. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
3. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

Academic Year 2016-17

16MVS202 - MIXED SIGNAL CIRCUIT DESIGN

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. PDC
2. LDICA

Course Objectives:

1. To import knowledge on different switched capacitor circuits.
2. To gain knowledge on filter design in mixed signal mode.
3. To gain knowledge on PLLs.
4. To understand different data converters (ADCs and DACs).
5. To acquire knowledge on Oversampling Converters.
6. To acquire knowledge on design different architectures in mixed signal mode.

Course Outcomes: At the end of the course the students will be able to

1. Analyze different switched capacitor circuits.
2. Design filters with different orders in mixed signal mode.
3. Categorize various PLLs.
4. Explain analyze different ADCs and DACs.
5. Explain the functioning of various modulators.

UNIT -I: Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II: Sample and Hold circuits: Performance requirements, MOS sample and hold basics, clock feed through problems, S/H using transmission gates, high input impedance S/H circuits, improved S/H circuits from the point of slewing time, clock feed through cancellations.

UNIT -III: Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT -IV: Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT -V: Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters. **Oversampling Converters:** Noise shaping modulators, Decimating filters and interpolating filters, higher order modulators, Delta sigma modulators with multi-bit quantizers, Delta sigma D/A Converters.

Text Books:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

Reference Books:

1. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013
2. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003.
3. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
4. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

Academic Year 2016-17

16MVS203 - VLSI AND DSP ARCHITECTURE
(Elective- V)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. DSP
2. VLSI Design

Course Objectives:

1. To know the various methods of implementation of DSP systems.
2. To impart knowledge on implementations of VLSI DSP architectures for Arithmetic operations
3. To know DSP systems and their applications.
4. To gain technical knowhow of DSP processors like TMS320 and SHARC processors

Course Outcomes: At the end of the Course students will be able to:

1. Distinguish the different methods used for Digital signal Processing.
2. State the implementation of DSP Systems using VLSI ICs
3. Explain the Applications of DSP systems
4. Compare the working of DSP systems like TMS320 and SHARC processors

UNIT I - Overview Of Digital Signal Processing: Advantages of DSP over analog systems, salient features and characteristics of DSP systems, applications of DSP systems. Common features of DSP processors, numeric representations in DSP processor, data path of a DSP processor, memory structures in DSP processors, VLIW architecture, special addressing modes in DSP processors, pipelining concepts, on-chip peripherals found in DSP processors.

UNIT II - Scaling And Roundoff Noise: Introduction to Scaling and Roundoff Noise- State Variable Description of Digital Filters- Scaling and Roundoff Noise Computation-Round Off Noise Computation Using State Variable Description- Slow-Down- Retiming and Pipelining.

UNIT III - Digital Multiplier Architectures: Parallel Multipliers- Interleaved Floor-plan and Bit-Plane-Based Digital Filters- Bit-Serial Multipliers- Bit-serial Filter Design and Implementation-Canonic Signed Digit Arithmetic- Distributed Arithmetic.

UNIT IV - Synchronous And Asynchronous Pipelining: Synchronous Pipelining and Clocking Styles- Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs- Wave Pipelining-Constraint Space Diagram and Degree of Wave Pipelining- Implementation of Wave-Pipelined Systems- Asynchronous Pipelining- Signal Transition Graphs- Use of STG to Design Interconnection Circuits- - Implementation of Computational Units.

UNIT V - TMS320 Processors And Sharc Processor: Architecture of TMS320C3X- Instruction Set- Addressing Modes- Data Formats- Floating Point Operation- Pipelining and Peripherals Architecture of TMS320C5X Processors- Assembly Instructions- Addressing

Modes- Pipelining and Peripherals. **SHARC PROCESSOR:** VLIW Architecture- SHARC- SIMD- MIMD Architectures- Application Adaptive filters-DSP based biometry receiver-speech processing-position control system for hard disk drive-DSP based power meter.

Text Books:

1. K.K Parhi: "VLSI Digital Signal processing", John-wiley, 2nd Edition Reprint, 2008.
2. Avatar Singh and S.Srinivasan, "Digital signal processing", Thomson books, 2004.

Reference Books:

1. John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India, 1st Edition, 2009.
2. B.Venkatramani & M.Baskar, "Digital Signal Processor", Tata McGraw Hill, 4th Edition, 2008.

Academic Year 2016-17

16MVS204 - CUSTOM IC DESIGN
(Elective- V)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. VLSI Design

Course Objectives:

1. To study different categories of ASIC arrays.
2. To learn ASIC PLA and PLD designs.
3. To study ASIC characteristics and performance.
4. To understand the design tools- FPGA Design tools: XILINX, ALTERA
5. To learn various Verilog and logic synthesis -VHDL and logic synthesis

Course Outcomes: At the end of the Course students will be able to:

1. Design and synthesize a complex digital functional block, containing over 1,000 gates using Verilog HDL and Synopsys Design Compiler.
2. Explain design flow and methodology- Hardware description languages-simulation
3. Demonstrate an understanding of issues involved in ASIC design, including technology choice, design management, tool
4. Explain flow, verification, debug and test, as well as the impact of technology scaling on ASIC design.
5. Implement & learn various ASIC construction packages.

UNIT I: ASIC Design Styles: Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs. ASICS – PROGRAMMABLE LOGIC DEVICES: Overview – PAL –based PLDs: Structures; PAL Characteristics – FPGAs: Intoduction, selected families – design outline.

UNIT II: ASICS –Design Issues: Design methodologies and design tools – design for testability – economies. ASIC Characteristics and Performance: design styles, gate arrays, standard cell -based ASICs, Mixed mode and analogue ASICs.

UNIT III: ASICS-Design Techniques: Overview- Design flow and methodology- Hardware description languages-simulation and checking-commercial design tools- FPGA Design tools: XILINX, ALTERA .

UNIT IV: Logic Synthesis, Simulation And Testing: Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation- automatic test pattern generation.

UNIT V: **ASIC Construction And FPGA Partitioning: ASIC Construction:** Floor planning, placement and routing system partition. **FPGA Partitioning**: Partitioning Methods-Floor

Planning- Placement-Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

Text Books:

1. L.J.Herbst,"Integrated circuit engineering", OXFORD SCIENCE Publications, 1996.
2. "VLSI Custom Microelectronics: Digital: Analog, and Mixed-Signal"-By Stanley L. Hurst-Marcel Dekker INc

Reference Books:

1. M.J.S.Smith, "Application - Specific integrated circuits", Addison-Wesley Longman 1997.
2. Variation-Aware Design of Custom Integrated Circuits: A Hands-on Field Guide-Trent McConaghy, Kristopher Breen, Jeffrey Dyck, Amit Gupta-Springer.
3. Signal Integrity Effects in Custom IC and ASIC Designs- Raminderpal Singh-Wiley-Blackwell

Academic Year 2016-17

16MVS205 - VLSI INTERCONNECTS AND DESIGN TECHNIQUES
(Elective- V)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. EMTL
2. Electric Circuits

Course Objectives:

1. To introduce the student to the fundamental theory and concepts of VLSI interconnects and transmission lines, and their practical applications.
2. To study the transmission line analysis for single, parallel and multilevel interconnections.
3. To provide the understanding of micro-strip line transmission.
4. To understand the differences between use of copper and other semiconductors as interconnects.
5. To analyze and design parallel interconnects in Micro-strip line.
6. To use the VLSI and optical interconnection concepts in Nano-tubes

Course Outcomes: Upon successful completion of the course students will be able to:

1. Differentiate and analyze different interconnects available in VLSI applications so that he/she will be able to use it for propagation in micro-strip.
2. Determine the interconnection delays for different interconnects, so that lossy and lossless micro-strip lines can be designed.
3. Analyze parallel – single and multilevel interconnects for Micro-strip line.
4. Apply the theory of Optical interconnects for carbon Nano tubes.
5. Analyze and determine the issues of crosstalk, to make the transmission line analysis simpler.
6. Design the parallel- single and multilevel interconnects for microstrip and other lossy transmissions.

UNIT –I: Preliminary Concepts Of VLSI Interconnects: Interconnects for VLSI applications- copper interconnections –method of images- method of moments- even and odd capacitances- transmission line equations- miller's theorem- Resistive interconnects as ladder network- Propagation modes in micro strip interconnects- slow wave propagations- Propagation delay.

UNIT – II: Parasitic Resistances, Capacitance And Inductances: Parasitic resistances, capacitances and inductances- approximate formulas for inductances- green's function method: using method of images and Fourier integral approach- network Analog method- Inductance extraction using fast Henry- copper interconnections for resistance modelling.

UNIT- III: Interconnection Delays: Metal insulator semiconductor micro strip line- transmission line analysis for single level interconnections- transmission line analysis for parallel multilevel interconnections- analysis of crossing interconnections

UNIT-IV: Cross Talk Analysis: Lumped capacitance approximation- coupled multi conductor MIS microstrip line model for single level interconnects- frequency domain level for single level interconnects- transmission line level analysis of parallel multilevel interconnections.

UNIT-V: Advanced Parallel Interconnects For Micro-Strip Line: Parallel interconnection models for micro strip line- modeling of lossy parallel and crossing interconnects- high frequency losses in micro strip line- Expressions for interconnection delays- Active interconnects. **Novel Solutions For Problems In Interconnects:** Optical interconnects – carbon Nano tubes / Graphenes vs. Copper wires.

Text Books:

1. H B Bakog Lu, Circuits, "Interconnections and packaging for VLSI",Addison Wesley publishing company.
2. J A Davis, J D Meindl, "Interconnect technology and design forGigascale integration", Kluwer academic publishers.

Reference Books:

1. Nurmi J, Tenhumen H, Isoaho J, Jantsch A, "Interconnect Centric deisgn for advanced SOC and NOC", Springer.
2. C K Cheng, J Lillis, S Lin, N Chang, "Interconnect analysis and synthesis", Wiley inter-science.
3. Hall S H, G W Hall and J McCall, High speed digital system design, Wiley inter-science
4. Askok K Goel, "High speed VLSI interconnections", Wiley interscience, second edition, 2007.

Academic Year 2016-17

16MVS206 - OPTIMIZATION TECHNIQUES IN VLSI DESIGN
(Elective- VI)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. PTSP
2. VLSI Design

Course Objectives:

1. To introduce the student to the fundamental theory and concepts of Statistical modeling Methodology and their applications.
2. To study the Genetic Algorithm of placement and routing for VLSI.
3. To provide insight in to geometric programming optimization techniques used for floor planning and gate sizing.
4. To make the students realize the problems using bayesian networks and monte-carlo methods.
5. To provide basic understanding of work-test generation procedures for Power estimation.
6. To provide knowledge of parameters to be determined such as STA, dynamic power, leakage power.

Course Outcomes: Upon successful completion of the course, students will be able to:

1. Differentiate and analyze different static modeling techniques and algorithms for VLSI, so that the student can determine the interconnect delays and performance.
2. Determine and estimate different parameters such as power, delay, performance and STA.
3. Work on geometric programming optimization applicable for gate sizing, wire sizing and floor planning.
4. Explain the importance of monte-carlo methods in probability
5. Compare different genetic algorithms and their applications such as layout and test automation and floor plan automation.
6. Analyze power estimation using the automation techniques

UNIT –I: Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgroms model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT – II: Statistical Performance, Power and Yield Analysis: Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT- III: Convex Optimization: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming

applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting-Monomial fitting, Maxmonomial fitting, Polynomial fitting.

UNIT-IV: Genetic Algorithm-I: Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology.

UNIT-V: Genetic Algorithm-II: Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding - local improvement - WDFR Comparison of CAS - Standard cell placement-GASP algorithm-unified algorithm. **GA Routing Procedures and Power Estimation:** Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATG problem encoding- fitness function-GA Vs Conventional algorithm.

Text Books:

1. "Statistical Analysis and Optimization for VLSI: Timing and Power" - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. "Genetic Algorithm for VLSI Design, Layout and Test Automation" - Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.

Reference Books:

1. "Convex Optimization", Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004.
2. "Algorithms for VLSI Design Automation",S H Gerez, Wiely Student Edition, John Wiley & Sons (Asia) (Pvt) Ltd.,1999.

Academic Year 2016-17

16MVS207 - SYSTEM ON CHIP ARCHITECTURE
(Elective- VI)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. Computer Organization
2. Embedded System Design.

Course Objectives:

1. To introduce the architectural features of system on chip.
2. To provides information on interconnection necessities between computational block and memory block.

Course Outcomes:

1. Introduction to SOC Architecture and design.
2. Processor design Architectures and limitations
3. To acquires the knowledge of memory architectures on SOC.
4. To understands the interconnection strategies and their customization on SOC.

UNIT –I: Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II: Processor: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III: Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV: Interconnect Architectures: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

UNIT -V:Interconnect Customization and Configuration: SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism. **Application Studies / Case Studies:** SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression

Text Books:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

Reference Books:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer.
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

Academic Year 2016-17

16MVS208 - SEMICONDUCTOR MEMORY DESIGN AND TESTING
(Elective- VI)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. VLSI Design

Course Objectives:

1. To provide knowledge on different types of RAMs such as SRAM and DRAM.
2. To provide knowledge on non volatile memories such as ROM, PROM, EPROM and EEPROM.
3. To give knowledge on memory fault modelling and testing.
4. To provide knowledge on semiconductor memory reliability and radiation effects.
5. To provide knowledge of Design and implementation of BiCMOS DRAMs
6. To provide knowledge on advanced memory technologies and high-density memory packing technologies.

Course Outcomes: Upon successful completion of the course, students will be able to:

1. Distinguish the different random access memory technologies operations and development using CMOS.
2. Categorize non volatile memories like ROM, PROM, EPROM and EEPROM.
3. Describe memory fault modelling and testing of RAMs and BIST techniques for memory.
4. Explain general reliability issues of RAM radiation testing and test structures.
5. Describe advanced memory technologies and high-density memory packing technologies testing and reliability issues.
6. Design and implement BiCMOS DRAMs.

UNIT-I: Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell.

UNIT-II: Advanced RAMs: Structures of BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-III: Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

UNIT –IV: Memory Fault Modeling and Testing: Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing,

IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory.

UNIT –V: Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures. Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

Text Books:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.

Reference Books:

1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

Academic Year 2016-17

16MVS209 - LOW POWER VLSI DESIGN
(Elective - VII)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. STLD
2. EDC
3. VLSI Design

Course objectives:

1. To make the students understand the requirement of low power ICs , designing of ICsfor low power dissipation
2. To make the student understand phenomena like short channel effect, punch through, surface scattering, velocity saturation, impact ionization, hot electron effect.
3. To make the student understand the low power design approches like voltage scaling using VTmos & MTmos circuits and architectural approaches like pipelining and parallel processing.
4. To make the student understand different types of adders like RCA,CSA,carry look ahead adder etc and also able to design adders with low power dissipation and low voltage operation.
5. To make the student different types of multipliers like booths multiplier and wallace tree multiplier.
6. To impart knowledge on functioning of ROMS ,SRAMS,DRAMS and power dissipation and consumption reduction methods in memory chips.

Course outcomes: At the end of the course the students will be able to:

1. Analyze the requirement of low power ICs and also able to understand the various power dissipation mechanisms like switching, short circuit, leakage etc.
2. Distinguish the phenomena like short-channel effect, punch through, surface scattering, velocity saturation, impact ionization, hot electron effect.
3. Explain the low power design approaches like voltage scaling using VTmos & MTmos circuits and architectural approaches like pipelining and parallel processing.
4. Distinguish different types of adders like RCA, CSA, carry look ahead adder etc and also able to design adders with low power dissipation and low voltage operation.
5. Compare different types of multipliers like booths multiplier and Wallace tree multiplier.
6. Explain the functioning of ROMS, SRAMS, DRAMS and power dissipation reduction methods adapted in three memory chips.

UNIT –I: Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation. Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity, Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II: Low-Power Design Approaches:
Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. **Switched Capacitance Minimization Approaches:** System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III: Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV: Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V: Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Text Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons,2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

Academic Year 2016-17

16MVS210 - DIGITAL HDL DESIGN AND VERIFICATION
(Elective - VII)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. STLD
2. DDVH

Course Objectives:

1. To introduce the student to the Basic concepts of Verilog.
2. To study the Verilog concepts like Tasks and Functions, Timing and delays, Switch level modeling.
3. To Study the System Verilog coding.
4. To understand the object oriented analysis in system Verilog
5. To understand the advanced features in System Verilog like Inter-processor synchronization - communication- scheduling semantics.

Course Outcomes: Upon successful completion of the course students will be able to:

1. Explain various programming concepts in Verilog.
2. Write program for Behavioral Simulation and Synthesis in Verilog.
3. Explain programming concepts in System Verilog.
4. Interpret the object oriented analysis in system Verilog.
5. Explain system Verilog assertion API and coverage API

UNIT –I: Verilog - Basic Concepts: Operators, Basic concepts, Identifiers, System task and functions, Value set, Data types, Parameters ,Operands, Operators, Modules and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling, Test bench.

UNIT-II: Verilog - Advanced Features: Tasks and Functions, Timing and delays, Switch level modeling, Tri state gates, MOS Switches, Bidirectional switches, User defined primitives, Combinational UDP, Sequential UDP, lab exercise. Introduction to synthesis,Verilog HDL synthesis-Synthesis Design flow –lab exercise.

UNIT-III: System Verilog – Introduction: Introduction to System Verilog – Literal values-data Types, Arrays, Data Declarations-attributes-operators, expressions, procedural statements and control flow. Processes in System Verilog – Task and functions.

UNIT-IV: Object Oriented Analysis In System Verilog: Introduction to objects, its properties, methods, constructors- casting – chaining - Data hiding and encapsulation – polymorphism. Random constraints – randomization method. Inline constraints, disabling random variables, controlling constraint, In-line random variable control-randomization of scope variable.

UNIT- V: System Verilog – Advanced Features: Inter-processor synchronization - communication- scheduling semantics-clocking blocks- assertions- Hierarchy-Interfaces- System Tasks & functions – system Verilog assertion API and coverage API.

Text Books:

1. Samir palnitkar, ”Verilog HDL”, Pearson education, Second Edition,20O3.
2. J. Bhasker, “A Verilog HDL Primer, Second Edition”, Star Galaxy, 1999.

Reference Books:

1. J. Bhasker, “A Verilog Synthesis: A Practical Primer”, Star Galaxy, 1998.
2. System Verilog 3.1a –Language Reference Manual (Accellera Extensions to Verilog 2001), 2004.

Academic Year 2016-17

16MVS211 - HIGH SPEED VLSI
(Elective - VII)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. STLD
2. VLSI Design

Course Objectives:

1. To provide different clocked logic analysis for different logic gates.
2. To provide knowledge on circuit design variations and margins.
3. To give knowledge on design of latches and racing conditions.
4. To provide knowledge on interfacing techniques between different chips.
5. To provide knowledge on different clocking styles.
6. To provide ability to design different interconnect depending on applications.

Course outcomes: At the end of the course the students will be able to:

1. Implement the clocked logic styles for different alternative logic gates.
2. Design induced variations and circuit design margining.
3. Realize basic latch design and different strategies.
4. Describe signaling standards, chip to chip communication networks.
5. Compare the different clocking styles including clock jitter, skew.
6. Design different interconnect depending on applications.

UNIT I: Clocked Logic Styles: Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked pass Gate Logic Non Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked pass Gate Families.

UNIT II: Circuit Design Margining And Design Variability: Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise.

UNIT III: Latching Strategies: Latching Strategies, Basic Latch Design, Latching Differential Logic, Race Free Latches for Pre-charged Logic, Asynchronous Latch Techniques.

UNIT IV: Interface Techniques: Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection, Skew Tolerant Design.

UNIT V: Clocking Styles: Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques. **PRELIMINARY CONCEPTS:** Interconnections for VLSI Applications, Metallic Interconnections - Multilevel, Multilayer and Multipath Configurations, Optical Interconnections, Superconducting Interconnections.

Text Books:

1. William S. Dally & John W. Poulton, “Digital Systems Engineering”, Cambridge University Press, 1998.

2. Howard Johnson & Martin Graham, "High Speed Digital Design" A Handbook of Black Magic, Prentice Hall PTR, 1993.

Reference Books:

1. Kerry Bernstein, Keith M. Carrig, *"High Speed CMOS Design Styles",* Kluwer Academic Publishers, 2002.
2. Evan Sutherland, Bob Stroll, David Harris," *Logical Efforts, Designing Fast CMOS Circuits",* Kluwer Academic Publishers, 1999
3. David Harris, *"Skew Tolerant Domino Design",* IEEE Journal of Solid State Circuits, 2001.

Academic Year 2016-17

16MVS212 - SCRIPTING LANGUAGES
(Elective - VIII)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. C Language Programming

Course Objectives: The goal of the course is to study:

1. The principles of scripting languages.
2. Motivation for and applications of scripting.
3. Difference between scripting languages and non- scripting languages.
4. Types of scripting languages.
5. Scripting languages such as PERL, TCL/TK, python and BASH.
6. Creation of programs in the Linux environment.
7. Usage of scripting languages in IC design flow.

Course Outcomes: Upon learning the course, the student will have the:

1. Ability to create and run scripts using PERL/TCl/Python in IC design flow.
2. Ability to use Linux environment and write programs for automation of scripts in VLSI tool design flow.

Unit – I : Linux Basics: Introduction to Linux , File System of the Linux, General usage of Linux kernel & basic commands, Linux users and group, Permissions for file, directory and users, searching a file & directory, zipping and unzipping concepts.

Unit – II : Linux Networking: Introduction to Networking in Linux, Network basics & Tools, File Transfer Protocol in Linux, Network file system, Domain Naming Services, Dynamic hosting configuration Protocol & Network information Services.

Unit – III : Perl Scripting: Introduction to Perl Scripting, working with simple values, Lists and Hashes, Loops and Decisions, Regular Expressions, Files and Data in Perl Scripting, References & Subroutines, Running and Debugging Perl, Modules, Object – Oriented Perl.

Unit – IV : Tcl / Tk Scripting: Tcl Fundamentals, String and Pattern Matching, Tcl Data Structures, Control Flow Commands, Procedures and Scope, Evel, Working with Unix, Reflection and Debugging, Script Libraries, Tk Fundamentals, Tk by examples, The Pack Geometry Manager, Binding Commands to X Events, Buttons and Menus, Simple Tk Widgets, Entry and List box Widgets Focus, Grabs and Dialogs.

Unit –V : Python Scripting: Introduction to Python, using the Python Interpreter, More Control Flow Tools, Data Structures, Modules, Input and Output, Errors and Exceptions, Classes, Brief Tour of the Standard Library.

Text Books:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Red Hat Enterprise Linux 4 : System Administration Guide Copyright, 2005 Red Hat Inc.

Reference Books:

1. Learning Python – 2nd Ed., Mark Lutz and David Ascher, 2003, O'Reilly.
2. Learning Perl – 4th Ed. Randal Schwartz, Tom Phoenix and Brain d foy. 2005.
3. Jython Essentials – Samuele Pedroni and Noel Pappin.2002. O'Reilly.
4. Python Tutorial by Guido Van Rossum, Fred L. Drake Jr. editor , Release 2.6.4
5. Practical Programming in Tcl and Tk by Brent Welch, Updated for Tcl 7.4 and Tk 4.0.

Academic Year 2016-17

16MVS213 - VLSI SIGNAL PROCESSING
(Elective - VIII)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. DSP
2. VLSI Design

Course Objectives: Students will be able to

1. Learn Pipelining, Parallel Processing and Retiming
2. Understand Folding and Unfolding
3. Analyze Systolic Architecture Design
4. Perform Fast Convolution
5. Understand Low Power Design techniques

Course Outcomes: Students will be able to

1. Apply Pipelining, Parallel Processing and Retiming for improving processing speed.
2. Demonstrate register minimization techniques using Folding and Unfolding methods.
3. Perform multiplication using Systolic Architecture.
4. Evaluate Convolution of signals using different algorithms.
5. Analyze architectures for Low Power consumption in multimedia signal processing.

UNIT -I: Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms. **Pipelining and Parallel Processing:** Introduction, Pipelining of FIR Digital filters, Parallel Processing, pipelining and Parallel Processing for Low Power. **Retiming:** Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques.

UNIT –II: Folding and Unfolding: Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems. **Unfolding:** Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding.

UNIT -III: Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays.

UNIT -IV: Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection.

UNIT -V: Low Power Design: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

Text Books:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

Reference Books:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.
3. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.

Academic Year 2016-17

16MVS214 - ADVANCED COMPUTER ARCHITECTURE
(Elective - VIII)

I Year – I Sem M. Tech

L	T	P	C
4	-	-	4

Pre-requisite(s):

1. Computer Organization and Operating System

Course Objectives:

1. Explains instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
2. Explains different classifications of instruction set architectures
3. Explains the advanced concepts such as instruction level parallelism, , out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction
4. Examine software support for ILP, including VLIW and similar approaches
5. Teach memory hierarchy design issues, including caching and virtual memory approaches
6. Explains multiprocessor and parallel processing architectures
7. Gives the organization and design of contemporary processor architectures
8. As the current trend in computer architecture is towards chip-multiprocessing, the architecture of shared memory multiprocessors and chip level interconnect (network-on-chip) will be covered as future scope.

Course Outcomes: A student who has met the objectives of the course will be able to:

1. Understand advanced computer architecture aspects
2. Describe and explain instruction level parallelism with static scheduling, out-of-order execution and network-on-chip architectures
3. Understand the architecture and limitations of chip-multiprocessing
4. Explain in detail about time-predictable computer architecture
5. Understand the operation of modern CPUs including pipelining, memory systems and busses.
6. Design and emulate a single cycle or pipelined CPU by given specifications using Hardware Description Language (HDL).
7. Write reports and make presentations of computer architecture projects

UNIT- I: Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set-memory addressing- type and size of operands, operations in the instruction set.

UNIT – II: Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties. **Memory Hierarchy Design:** Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III: Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV: Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V: Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. **Intel Architecture:** Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls.

Text Books:

1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.
2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs., MC Graw Hill.

Reference Books:

1. John P. Shen and Miikko H. Lipasti, Modern Processor Design : Fundamentals of Super Scalar Processors.
2. Advanced Computer Architecture - A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk ,Pearson ed.

Academic Year 2016-17

16MVS2L1 - VLSI Lab – II

I Year – I Sem M. Tech

L	T	P	C
-	-	4	2

Pre-requisite(s):

1. VLSI Design
2. EDC
3. ECA.

Lab Objectives: Students will be able to

1. Draw Schematics for basic CMOS gates.
2. Analyze Transient and DC behaviour of different gates.
3. Understand the Layout Design Rules and apply the same to different gates.
4. Write SPICE code for different Analog circuits.
5. Perform AC analysis for different Analog circuits.

Lab Outcomes: Students will be able to

1. Design schematics for basic CMOS logic gates.
2. Apply design rules for Layout Development of CMOS circuits.
3. Develop and simulate SPICE code for Analog circuits.
4. Interpret the simulation results of Analog / Digital circuits.
5. Contrast DC/AC/Transient responses of Analog circuits.

VLSI Back End Design programs:

The design shall include Transistor-level design/Gate-level design/Hierarchical design. Simulation and Verification, Scaling of CMOS Inverter for different technologies, Circuit optimization with respect to area, performance and/or power, Layout, Extraction of Parasitics and back annotation, DC/Transient Analysis, Verification of Layouts (DRC, LVS) of the following:

1. Introduction to Layout Design Rules
2. Schematic and Layout of the following with analysis
    - CMOS Inverter
    - CMOS NOR/ NAND gates
    - CMOS XOR / MUX
    - CMOS Full Adder
    - Latch
    - Pass transistor
3. Layout of any AOI and OAI based combinational logic circuit
4. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
5. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
6. Analog Circuit simulation (AC analysis) - CS & CD amplifier
7. System level design using PLL

Note:- All the above digital / analog circuits are to be designed and implemented using Cadence /Mentor Graphics / Synopsys / Equivalent CAD tools.

Academic Year 2016-17

16MEN2SS- SOFT SKILLS
(Activity-based)

M.Tech. I Year II-Sem

L	T	P	C
-	-	4	2

Course Objectives

1. To improve the fluency of students in English
2. To facilitate learning through interaction
3. To illustrate the role of skills in real-life situations with case studies, role plays etc.
4. To train students in group dynamics, body language and various other activities which boost their confidence levels and help in their overall personality development
5. To encourage students develop behavioral skills and personal management skills
6. To impart training for empowerment, thereby preparing students to become successful professionals

Course Outcomes

CO1. Developed critical acumen and creative ability besides making them industry- ready.
CO2. Appropriate use of English language while clearly articulating ideas.
CO3. Developing insights into Language and enrich the professional competence of the students.
CO4. Enable students to meet challenges in job and career advancement.

INTRODUCTION

- Definition and Introduction to Soft Skills – Hard Skills vs Soft Skills – Significance of Soft/Life/Self Skills – Self and SWOT Analysis ***and***

1. Exercises on Productivity Development

- Effective/ Assertive Communication Skills (Activity based)
- Time Management (Case Study)
- Creativity & Critical Thinking (Case Study)
- Decision Making and Problem Solving (Case Study)
- Stress Management (Case Study)

2. Exercises on Personality Development Skills

- Self-esteem (Case Study)
- Positive Thinking (Case Study)
- Emotional Intelligence (Case Study)

- Team building and Leadership Skills (Case Study)
- Conflict Management (Case Study)

3. Exercises on Presentation Skills

- Netiquette
- Importance of Oral Presentation – Defining Purpose- Analyzing the audience- Planning Outline and Preparing the Presentation- Individual & Group Presentation- Graphical Organizers- Tools and Multi-media Visuals
- One Minute Presentations (Warming up)
- PPT on Project Work- Understanding the Nuances of Delivery- BodyLanguage – Closing and Handling Questions – Rubrics for IndividualEvaluation (Practice Sessions)

4. Exercises on Professional Etiquette and Communication

- Role-Play and Simulation- Introducing oneself and others, Greetings, Apologies, Requests, Agreement & Disagreement….etc.
- Telephone Etiquette
- Active Listening
- Group Discussions (Case study)- Group Discussion as a part of Selection Procedure- Checklist of GDs
- Analysis of Selected Interviews (Objectives of Interview)
- Mock-Interviews (Practice Sessions)
- Job Application and Preparing Resume
- Process Writing (Technical Vocabulary) – Writing a Project Report- Assignments

5. Exercises on Ethics and Values

- Introduction — Types of Values - Personal, Social and Cultural Values - Importance of Values in Various Contexts
- Significance of Modern and Professional Etiquette – Etiquette (Formal and Informal Situations with Examples)
  - Attitude, Good Manners and Work Culture (Live Examples)
  - Social Skills - Dealing with the Challenged (Live Examples)
  - Professional Responsibility – Adaptability (Live Examples)
  - Corporate Expectations
- Note: Hand-outs are to be prepared and given to students.
- Training plan will be integrated in the syllabus.
- Topics mentioned in the syllabus are activity-based.

SUGGESTED SOFTWARE:

- The following software from **'train2success.com'**
- Preparing for being Interviewed
- Positive Thinking
- Interviewing Skills
- Telephone Skills
- Time Management
- Team Building
- Decision making

SUGGESTED READING:

1. Alex, K. 2012. Soft Skills. S. Chand Publishers
2. Management Shapers. 2011. Collection of 28 Books by different Authors. Universities Press.
3. Sherfield, Robert M. 2005. et al Cornerstone: Developing Soft Skills. Pearson
4. Suresh Kumar,E; Sreehari, P. & Savithri, J. 2011. Communication Skills and Soft Skills-An Integrated Approach. New Delhi: Pearson
5. The ACE of Soft Skills by Gopalaswamy Ramesh & Mahadevan Ramesh. 2013. Pearson Publishers. New Delhi.
6. Patnaik, P. 2011. Group Discussion and Interview Skills. New Delhi: Foundation
7. Sudhir Andrews. 2009. How to Succeed at Interviews. New Delhi: Tata McGraw Hill
8. **Sasikumar, V & Dhamija, P.V. 1993. Spoken English - A Self-Learning Guide to Conversation Practice. New Delhi: Tata McGraw-Hill**
9. Dixso, Richard J. Everyday Dialogues in English. Prentice Hall India Pvt Ltd
10. Mukhopadhyay. L et al. 2012. Polyskills. New Delhi: CUP India Pvt Ltd
11. Rizvi, M. A. 2005. Effective Technical Communication. New Delhi: Tata McGraw Hill
12. The Hindu Speaks on Education by the Hindu Newspaper
13. Naterop, B. Jean and Revell, Rod. 2004. Telephoning in English. Cambridge: CUP